

**AMENDMENTS TO THE CLAIMS**

1-24. (Cancelled)

25. (Currently Amended) A method for forming an asymmetric insulating layer for a volatile memory structure, comprising the steps of:

providing a substrate having a pair of neighboring trenches;

forming a buried trench capacitor in a lower portion of each trench;

forming an asymmetric collar insulating layer, having a high level portion and a low level portion, over an upper portion of the sidewall of each trench, and forming a conductor layer, overlying the buried trench capacitor in each trench, below the upper surface of the substrate with a lower part of the conductive layer surrounded by the asymmetric collar insulating layer, wherein the high level portion of the asymmetric collar insulating layer is adjacent to the substrate between the neighboring trenches and the low level portion is covered by an upper part of the conductive layer, wherein the step of forming the asymmetric collar insulating layer comprises:

forming a sacrificial layer in each trench, the sacrificial layer overlying the buried trench capacitor ~~in each trench and being~~ surrounded by an insulating spacer protruding the surface of the sacrificial layer;

covering portions of the insulating spacers adjacent to the substrate between the neighboring trenches by a masking layer;

removing the uncovered insulating spacers to form the asymmetric collar insulating layer; and

successively removing the masking layer and the sacrificial layer;

forming a dielectric layer overlying the conductive layer in each trench; and

forming two access transistors on the substrate outside of the pair of the neighboring trenches, respectively, wherein the two access transistors have source/drain regions electrically connecting to the conductive layer.

26. (Previously Presented) The method as claimed in claim 25, wherein the sacrificial layer is a photoresist or anti-reflection layer.

27. (Previously Presented) The method as claimed in claim 25, wherein the masking layer is a photoresist layer.

28. (Previously Presented) The method as claimed in claim 25, wherein the conductive layer is a doped polysilicon layer.

29. (Previously Presented) The method as claimed in claim 25, wherein before the step of forming the dielectric layer, further comprises:

forming active area/isolation areas through an active area masking layer.

30. (Previously Presented) The method as claimed in claim 29, wherein the active area masking layer is a strap type pattern.

31. (Currently Amended) A method for forming a trench capacitor structure for a volatile memory device, comprising the steps of:

providing a substrate having a trench;

forming a buried bottom plate in the substrate around a lower portion of the trench;

forming a capacitor dielectric layer over a lower portion of the sidewall of the trench ;

forming a top plate in the trench and surrounded by the capacitor dielectric layer;

forming an asymmetric collar oxide layer, having a high level portion and a low level portion, over an upper portion of the sidewall of the trench, and forming a conductive layer, overlying the top plate in the trench, below the upper surface of the substrate with a lower part of the conductive layer surrounded by the asymmetric collar oxide layer, wherein the low level portion of the asymmetric collar oxide layer is covered by an upper part of the conductive layer, wherein the step of forming the asymmetric collar oxide layer comprises:

forming a sacrificial layer in the trench, the sacrificial layer overlying the top plate in the trench and being surrounded by an oxide spacer protruding the surface of the first masking layer;

covering a portion of the oxide spacer by a masking layer;

removing the uncovered oxide spacer to form the asymmetric collar oxide layer; and

successively removing the masking layer and the sacrificial layer; and

forming a dielectric layer overlying the conductive layer in the trench.

32. (Previously Presented) The method as claimed in claim 31, wherein the sacrificial layer is a photoresist or anti-reflection layer.

33. (Previously Presented) The method as claimed in claim 31, wherein the masking layer is a photoresist layer.

34. (Previously Presented) The method as claimed in claim 31, wherein the conductive layer is a doped polysilicon layer.

35. (Previously Presented) The method as claimed in claim 31, wherein before the step of forming the dielectric layer, further comprises:

forming active area/isolation areas through an active area masking layer.

36. (Previously Presented) The method as claimed in claim 35, wherein the active area masking layer is a strap type pattern.